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Following Paper ID and Roll No. to be filled in your Answer Book.

PAPER ID : 43206 Roll No. 1 2 3 0 4 3 2 0 1 1

B. Tech. Examination, 2024-25

(Odd Semest

DIGITAL LOGIC DESIGN

Time : Three Hours] *[Maximum Marks : 60*

Note :– Attempt all questions.

SECTION–A

1. Attempt all parts of the following : 8×1=8

(a) What is gray code? Give the advantage of gray code over binary code.

(b) Find the standard SoP form of the following fucntion :

$$f(A, B, C, D) = \bar{A} + B C \bar{D} + A \bar{C}$$

(c) What do you mean by sign-magnitude representation?

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(d) What are the different hazards in combinational circuits?

(e) Implement the following function using a multiplexer :

$$Y(A, B, C) = \Sigma m(1, 2, 5, 6)$$

(f) Explain the difference between asynchronous and synchronous sequential circuits.

(g) What are programmable logic devices?

(h) What is the significance of state assignment?

SECTION – B

2. Attempt any two parts of the following : 2×6=12

(a) Minimize the following Boolean function using K-map :

(i) $Y(A, B, C, D) = \Sigma m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$

(i) $Y(A, B, C, D) = \pi_M(1, 2, 3, 8, 9, 10, 11, 14) \cdot d(7, 15)$

(b) Implement the following combinational logic circuits using multiplexer :

(i) Half adder

(ii) Half subtractor

(c) Draw the logic circuit of J-K flip-flop using D-flip flop.

(d) Design a Mod-5 synchronous counter using T-flip flop.

SECTION – C

Note :– Attempt all questions. Attempt any two parts from each questions. 8×5=40

3. (a) Explain with example, how Hamming code is useful for detecting and correcting error in digital data transmission?

(b) Realize the following expression using EX-NOR gates :

$$f = \overline{A}\,B\,\overline{C}\,\overline{D} + A\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D + A\,B\,\overline{C}\,D$$

(c) Simplify the following four-variable Boolean function using Quine-McCluskey method :

$$Y(A, B, C) = \Sigma m(2, 4, 5, 9, 12, 13)$$

4. (a) Design a 4-bit binary-to-gray code converter using truth table, K-map and logic circuits.

(b) Describe the difference between PLA and PAL.

(c) Design a 4-bit odd parity generator using suitable gates.

5. (a) What is race-around condition? How does it get eliminated in a master-slave JK-flip flop? Explain.

(b) Design a Mod-9 ripple counter using T-flip-flop.

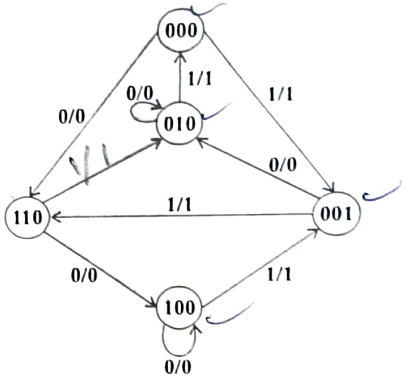
(c) Design a sequential generator using JK-flip-flop to generate the sequence :

$$0 \rightarrow 2 \rightarrow 4 \rightarrow 5 \rightarrow 1 \rightarrow 7 \rightarrow 6$$

6. (a) Describe the design procedure for asynchronous sequential circuits.

(b) Ekxplain the methods to eliminate static hazards in an asynchronous circuit. Also define races in asynchronous sequential circuits.

(c) Implement the following state diagram using D-flip flop :



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